CLAIMS

1. A variable-gain amplifier comprising:

a plurality of dual-gate FETs having first FETs having respective gates for being supplied with an input signal and second FETs having respective sources connected respectively to drains of the first FETs, the first FETs having respective sources connected in common to each other and the second FETs having respective drains connected in common to each other; and

a plurality of voltage control means connected to respective gates of the second FETs for applying gate voltages separately thereto.

2. A variable-gain amplifier comprising:

a plurality of variable-gain amplifying elements having FETs having respective gates for being supplied with an input signal and bipolar transistors having respective emitters connected respectively to drains of the FETs, the FETs having respective sources connected in common to each other and the bipolar transistors having respective collectors connected in common to each other; and

a plurality of voltage control means connected to respective bases of the bipolar transistors for applying base voltages separately thereto.

3. The variable-gain amplifier according to claim 1 or 2, wherein the FETs for being supplied with the input signal have substantially identical electric characteristics.

4. The variable-gain amplifier according to claim 1 or 2, wherein at least one of the FETs for being supplied with the input signal has electric characteristics different from electric characteristics of the other one or more of the FETs for being supplied with the input signal.

5. The variable-gain amplifier according to claim 1 or 2, further comprising a voltage feedback path interconnecting a signal input section and a signal output section.

6. A variable-gain amplifier comprising:

a plurality of first dual-gate FETs having first FETs having respective gates for being supplied with an input signal and second FETs having respective sources connected respectively to drains of the first FETs, the first FETs having respective sources connected in common to each other and the second FETs having respective drains connected in common to each other;

a plurality of second dual-gate FETs having third FETs having respective gates for being supplied with an

inverted input signal and fourth FETs having respective sources connected respectively to drains of the third FETs, the third FETs having respective sources connected in common to each other and the fourth FETs having respective drains connected in common to each other; and

a plurality of voltage control means connected to respective gates of the second FETs and respective gates of the fourth FETs for applying gate voltages separately thereto;

wherein the number of the first dual-gate FETs, the number of the second dual-gate FETs, and the number of the voltage control means are equal to each other.